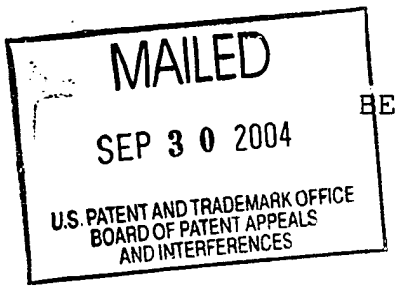
Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE



BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte THEODORE W. HOUSTON

Appeal No. 2004-2158
Application No. 09/346,436

ON BRIEF

Before KIMLIN, PAK and KRATZ, Administrative Patent Judges.

KIMLIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 9 and 22. Claims 25 and 26, the other claims remaining in the present application, have been objected to by the examiner (appellant's Substitute Supplemental Appeal Brief of October 23, 2002 states that "all claims have been canceled by not having been appealed with the exception of claims 9 and 22, which remain on appeal and claims 25 and 26 which have been stated to be allowable . . ." (page 1)). However, we note that appealed claims 9 and 22 depend

on cancelled claims 7 and 18, respectively. For purposes of this appeal, we will consider claims 9 and 22 to contain all the limitations recited in claims 7 and 18, respectively. Cancelled claims 7 and 18, as well as appealed claims 9 and 22, are reproduced below:

7. A method of forming an SOI structure, comprising the steps of:

providing a device layer having at least one of active or passive elements on a surface thereof;

providing a substrate having at least one of active or passive elements on a surface thereof;

providing an electrically insulating layer having an interconnect structure disposed therein and extending to a surface thereof;

forming a substantially planar region on said surface of said device layer and said surface of said substrate;

forming a substantially planar region on said surface of said electrically insulating layer;

interposing said electrically insulating layer between said device layer and said substrate with said planar region of said electrically insulating layer overlaying said substantially planar region on said at least one of said surface of said device layer and said surface of said substrate to make electrical contact with a device in at least one of the device wafer and the substrate; and

then bonding said planar surface of said electrically insulating layer to said overlying one of said substrate and said device layer.

9. The method of claim 7 further including the step of forming an electrical interconnect structure in said electrically

insulating layer, said interconnect structure contacting both said device layer and said substrate.

18. A method of fabricating an integrated circuit which comprises the steps of:

(a) providing a device layer having at least one of active or passive elements on a surface thereof;

(b) providing a substrate having at least one of active or passive elements on a surface thereof;

(c) providing a dielectric bonded to one of said device layer and said substrate having an interconnect disposed therein and extending to at least one surface thereof;

(d) then bonding said dielectric to the other of said device layer and said substrate to form an interface with said one of said device layer and said substrate and forming an electrically conductive path across said interface to said interconnect.

22. The method of claim 18, further including a dielectric disposed over said interconnect at said interface preventing electrical conduction across said interface, wherein said step of forming an electrically conductive path across said interface to said interconnect is formed by breakdown of said dielectric.

In addition to the admitted prior art found in appellant's specification, the examiner relies upon the following reference in the rejection of the appealed claims:

Hayashi	5,087,585	Feb. 11, 1992

Appellant's claimed invention is directed to a method of forming silicon on insulator (SOI) structures comprising, inter alia, forming an electrical interconnect structure in an insulating layer between a device layer and a substrate that has at least one active or passive element on its surface.

Appealed claim 9 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Hiyashi. Claim 22 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hiyashi in view of the admitted prior art set forth at page 7 of the instant specification.

We have thoroughly reviewed each of appellant's arguments for patentability. However, we are in complete agreement with the examiner that the claimed subject matter is unpatentable over the cited prior art. Accordingly, we will sustain the examiner's rejections for the reasons set forth in the Answer, which we incorporate herein, and we add the following for emphasis only.

Regarding the examiner's § 102 rejection of claim 9 over Hiyashi, appellant's principal contention is that interconnect 18 "of Hiyashi is disposed in an opening formed in the electrically insulating layer 17" but, somehow, "is not disposed in the electrically insulating layer" (see page 2 of Substitute Supplemental Appeal Brief, last two sentences). However, like the examiner, we do not understand how the interconnect of Hiyashi, which is admittedly disposed in an opening formed in the insulating layer, does not meet the claim 9 requirement of "forming an electrical interconnect structure in said electrically insulating layer."

Appellant also maintains that contact in Hiyashi is only made when refractory metal bump 13 contacts interconnect 18 and, therefore, "the order of the steps as specifically claimed in the combination of claims 7 and 9 is not met by Hiyashi" (page 3 of Substitute Supplemental Appeal Brief, first paragraph). However, we fully concur with the examiner that "[t]here exists no requirement in claims 7 or 9 as to when such contact is made or as to what type of contact, the claim limitation 'contact' is directed" (page 16 of Answer, second paragraph). Claim 9 simply recites "further including the step of forming an electrical interconnect . . ." without specifying when this further step occurs in the order of steps recited in cancelled claim 7. We also agree with the examiner that there is no apparent distinction between the order of steps disclosed by Hiyashi and those disclosed in the present specification.

Concerning the § 103 rejection of claim 22, appellant submits that "there is no so-called admission in Appellant's Admitted Prior Art (APA) that it is even known that the oxide will always appear in the process as claimed, let alone that it be known to remove such oxide, especially in the environment as claimed" (page 3 of Substitute Supplemental Appeal Brief,

paragraph three). As emphasized by the examiner, appellant's specification, at page 7, first paragraph, states the following:

> In the event a thin native oxide has developed over the device wafer 5 or the substrate 1 or the flowable dielectric insulates the interconnect in the electrically insulating layer from the substrate or device wafer, a sufficiently high voltage can be passed through the circuitry involving the interconnect 7 to cause breakdown of the native oxide or other dielectric and allow completion of the connection as is well known in the art [emphasis added].

Manifestly, it cannot be gainsaid that appellant's specification clearly states that it was known in the art to employ a high voltage to cause breakdown of any native oxide or other dielectric formed over the device wafer or substrate. If it is appellant's argument that there is no admission that the native oxide always appears, appellant, nonetheless, has not addressed the thrust of the examiner's rejection, namely, that it would have been obvious for one of ordinary skill in the art to employ the admittedly known technique of submitting the structure to a high voltage to cause breakdown of the native oxide or other dielectric when it occurs. Appellant has presented no argument why it would have been nonobvious to one of ordinary skill in the art to perform the "breakdown" step of claim 22.

As a final point with respect to the § 103 rejection, we observe that appellant bases no argument upon objective evidence

of nonobviousness, such as unexpected results, which would serve to rebut the prima facie case of obviousness established by the examiner.

In conclusion, based on the foregoing and the reasons well-stated by the examiner, the examiner's decision rejecting the appealed claims is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

EDWARD C. KIMLIN)
Administrative Patent Judge)
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CHUNG K. PAK) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
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